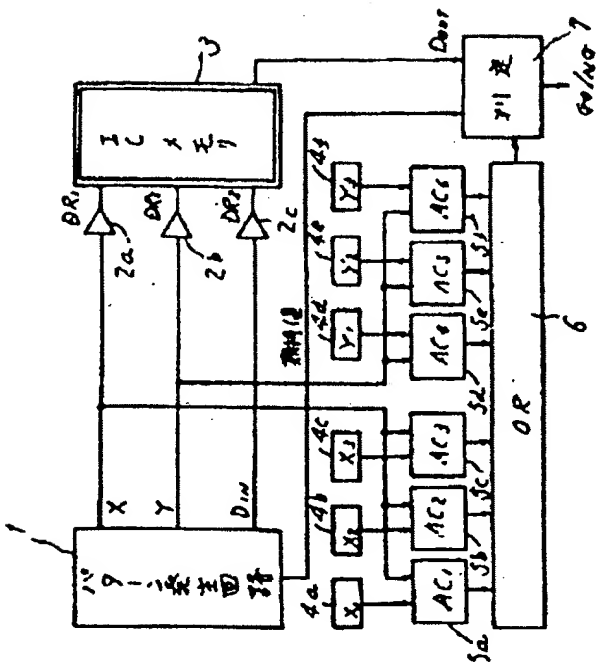
P A T E N T
A B S T R A C T S
O F
J A P A N



PUBLICATION NUMBER : 58155599

ABS-PUBL = 831210
ABS-VOL = 007-278
APPL-DAT = 820310
APPL-NUM = 57036426
FIR-PUBL = 830916
GROUP = P242
APPLICANT HITACHI SEISAKUSHO KK
INVENTOR WADA EIJI

IPC G11C29\00 H01L21\66 H01L27\10

TITLE MEMORY TESTER

ABSTRACT PURPOSE : To simplify the constitution of a memory tester, by generating a mask signal deciding a non-defective component forcedly, in response to the coincidence between an address signal and a defective address signal from a pattern generating circuit.
CONSTITUTION : An IC memory 3 provided with a redundant memory is accessed with line addresses X, Y from the pattern generating circuit 1, and the content written with a write signal DIN is read out. The content of readout Dout and an expected value from the circuit 1 are compared at a deciding circuit 7 for the test of the memory 3. In this case, the addresses X, Y and defective line addresses of registers 4a, 4b... are compared at comparators AC1, AC2..., a coincident output from the comparators AC1... via an OR circuit 6 is impressed to the circuit 7 as the mask signal, and at the accessing of the defective line, the result is decided to be a non-defective component forcedly and the next test is continued immediately. With the system making unnecessary the mask information memory to have the same capacity as the memory to be tested, the constitution of the memory tester is simplified.

END OF DOCUMENT